Distributed by:

JAMECO® ELECTRONICS

**www.Jameco.com ✦ 1-800-831-4242**

The content and copyrights of the attached material are the property of its owner.

Jameco Part Number 235281



FAIRCHILD SEMICONDUCTOR™

September 1988
Revised November 1999

# 74AC574 • 74ACT574
# Octal D-Type Flip-Flop with 3-STATE Outputs

## General Description

The AC/ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D-type inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The AC/ACT574 is functionally identical to the AC/ACT374 except for the pinouts.

## Features

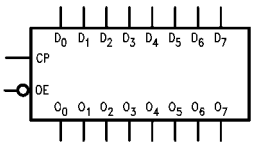
- $I_{CC}$ and $I_{OZ}$ reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to AC/ACT374
- 3-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- ACT574 has TTL-compatible inputs

## Ordering Code:

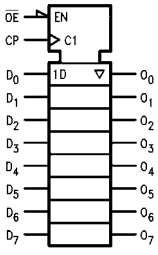
| Order Number | Package Number | Package Description |
|---|---|---|
| 74AC574SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body |
| 74AC574SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC574MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC574PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74ACT574SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-01 |
| 74ACT574SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ACT574MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT574PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

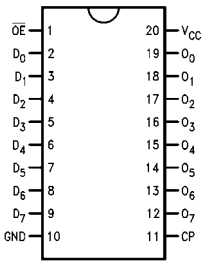
## Logic Symbols




**IEEE/IEC**




## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| CP | Clock Pulse Input |
| $\overline{OE}$ | 3-STATE Output Enable Input |
| $O_0$–$O_7$ | 3-STATE Outputs |

FACT™ is a trademark of Fairchild Semiconductor Corporation.

© 1999 Fairchild Semiconductor Corporation 

## Functional Description

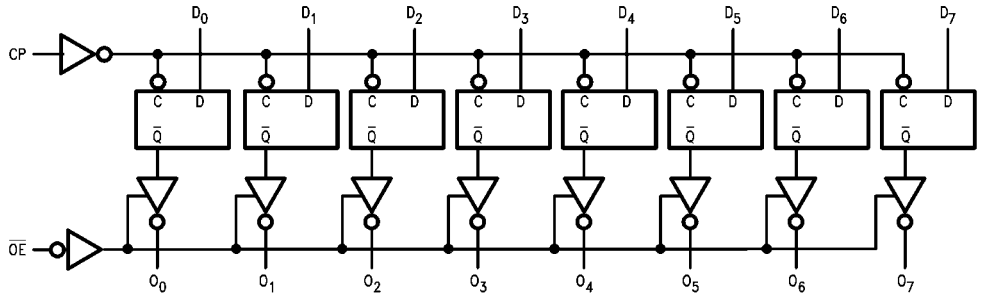
The AC/ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

## Function Table

| Inputs | | | Internal | Outputs | Function |
|---|---|---|---|---|---|
| $\overline{OE}$ | CP | D | Q | $O_N$ | |
| H | H | L | NC | Z | Hold |
| H | H | H | NC | Z | Hold |
| H | ↗ | L | L | Z | Load |
| H | ↗ | H | H | Z | Load |
| L | ↗ | L | L | L | Data Available |
| L | ↗ | H | H | H | Data Available |
| L | H | L | NC | NC | No Change in Data |
| L | H | H | NC | NC | No Change in Data |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ +0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ +0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ +0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ +0.5V |
| DC Output Source | |
| or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current | |
| Per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Junction Temperature ($T_J$) | |
| PDIP | 140°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| AC | 2.0V to 6.0V |
| ACT | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate (ΔV/Δt) | |
| AC Devices | |
| $V_{IN}$ from 30% to 70% of $V_{CC}$ | |
| $V_{CC}$ @ 3.3V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate (ΔV/Δt) | |
| ACT Devices | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = 25°C Typ | $T_A$ = −40°C to +85°C Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum HIGH Level | 3.0 | 1.5 | 2.1 | 2.1 | | $V_{OUT}$ = 0.1V |
| | Input Voltage | 4.5 | 2.25 | 3.15 | 3.15 | V | or $V_{CC}$ − 0.1V |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | |
| $V_{IL}$ | Maximum LOW Level | 3.0 | 1.5 | 0.9 | 0.9 | | $V_{OUT}$ = 0.1V |
| | Input Voltage | 4.5 | 2.25 | 1.35 | 1.35 | V | or $V_{CC}$ − 0.1V |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | |
| $V_{OH}$ | Minimum HIGH Level | 3.0 | 2.99 | 2.9 | 2.9 | | |
| | Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT}$ = −50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | 3.0 | | 2.56 | 2.46 | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | | 3.86 | 3.76 | V | $I_{OH}$ = −12 mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH}$ = −24 mA $I_{OH}$ |
| | | | | | | | $I_{OH}$ = −24 mA (Note 2) |
| $V_{OL}$ | Maximum LOW Level | 3.0 | 0.002 | 0.1 | 0.1 | | |
| | Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$or $V_{IH}$ |
| | | 3.0 | | 0.36 | 0.44 | | $I_{OL}$ = 12 mA |
| | | 4.5 | | 0.36 | 0.44 | V | $I_{OL}$ = 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL}$ = 24 mA (Note 2) |
| $I_{IN}$ (Note 4) | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OZ}$ | Maximum | | | | | | $V_I$ (OE) = $V_{IL}$, $V_{IH}$ |
| | 3-STATE | 5.5 | | ±0.25 | ±2.5 | μA | $V_I$ = $V_{CC}$, $V_{GND}$ |
| | Leakage Current | | | | | | $V_O$ = $V_{CC}$, GND |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V |
| $I_{OHD}$ | Output Current (Note 3) | 5.5 | | | −75 | mA | $V_{OHD}$ = 3.85V |
| $I_{CC}$ (Note 4) | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** $I_{IN}$ and $I_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{CC}$.

## DC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = 25°C$ Typ | $T_A = -40°C$ to $+85°C$ Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | |
| $V_{OH}$ | Minimum HIGH Level | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT} = -50\ \mu A$ |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | | 3.86 | 3.76 | V | $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24$ mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH} = -24$ mA (Note 5) |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT} = 50\ \mu A$ |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | | 0.36 | 0.44 | V | $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24$ mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL} = 24$ mA (Note 5) |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | µA | $V_I = V_{CC}$, GND |
| $I_{OZ}$ | Maximum 3-STATE Leakage Current | 5.5 | | ±0.25 | ±2.5 | µA | $V_I = V_{IL}$, $V_{IH}$ $V_O = V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I = V_{CC} - 2.1V$ |
| $I_{OLD}$ | Minimum Dynamic Output Current (Note 6) | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ |
| $I_{OHD}$ | | 5.5 | | | −75 | mA | $V_{OHD} = 3.85V$ |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | µA | $V_{IN} = V_{CC}$ or GND |

**Note 5:** All outputs loaded; thresholds on input associated with output under test.

**Note 6:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics for AC

| Symbol | Parameter | $V_{CC}$ (V) (Note 7) | $T_A = +25°C$, $C_L = 50$ pF Min | Typ | Max | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | 3.3 | 75 | 112 | | 60 | | MHz |
| | | 5.0 | 95 | 153 | | 85 | | |
| $t_{PLH}$ | Propagation Delay CP to $O_n$ | 3.3 | 3.5 | 8.5 | 13.5 | 3.5 | 15.0 | ns |
| | | 5.0 | 2.0 | 6.0 | 9.5 | 2.0 | 11.0 | |
| $t_{PHL}$ | Propagation Delay CP to $O_n$ | 3.3 | 3.5 | 7.5 | 12.0 | 3.5 | 13.5 | ns |
| | | 5.0 | 2.0 | 5.5 | 8.5 | 2.0 | 9.5 | |
| $t_{PZH}$ | Output Enable Time | 3.3 | 2.5 | 7.0 | 11.0 | 2.5 | 12.0 | ns |
| | | 5.0 | 2.0 | 5.0 | 8.5 | 2.0 | 9.0 | |
| $t_{PZL}$ | Output Enable Time | 3.3 | 3.0 | 6.5 | 10.5 | 3.0 | 11.5 | ns |
| | | 5.0 | 2.0 | 5.0 | 8.0 | 1.5 | 9.0 | |
| $t_{PHZ}$ | Output Disable Time | 3.3 | 3.5 | 7.5 | 12.0 | 2.5 | 13.0 | ns |
| | | 5.0 | 2.0 | 6.0 | 9.5 | 1.5 | 10.5 | |
| $t_{PLZ}$ | Output Disable Time | 3.3 | 2.0 | 5.5 | 9.0 | 1.5 | 10.0 | ns |
| | | 5.0 | 1.0 | 4.5 | 7.5 | 1.0 | 8.5 | |

**Note 7:** Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements for AC

| Symbol | Parameter | $V_{CC}$ (V) (Note 8) | $T_A = +25°C$, $C_L = 50$ pF | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_S$ | Set-Up Time, HIGH or LOW | 3.3 | 0.5 | 2.5 | 3.0 | ns |
| | $D_n$ to CP | 5.0 | 0 | 1.5 | 2.0 | |
| $t_H$ | Hold Time, HIGH or LOW | 3.3 | −0.5 | 1.5 | 1.5 | ns |
| | $D_n$ to CP | 5.0 | 0 | 1.5 | 1.5 | |
| $t_W$ | CP Pulse Width | 3.3 | 3.5 | 6.0 | 7.0 | ns |
| | HIGH or LOW | 5.0 | 2.0 | 4.0 | 5.0 | |

**Note 8:** Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

## AC Electrical Characteristics for ACT

| Symbol | Parameter | $V_{CC}$ (V) (Note 9) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | 5.0 | 100 | 110 | | 85 | | ns |
| $t_{PLH}$ | Propagation Delay CP to $O_n$ | 5.0 | 2.5 | 7.0 | 11.0 | 2.0 | 12.0 | ns |
| $t_{PHL}$ | Propagation Delay CP to $O_n$ | 5.0 | 2.0 | 6.5 | 10.0 | 1.5 | 11.0 | ns |
| $t_{PZH}$ | Output Enable Time | 5.0 | 2.0 | 6.4 | 9.5 | 1.5 | 10.0 | ns |
| $t_{PZL}$ | Output Enable Time | 5.0 | 2.0 | 6.0 | 9.0 | 1.5 | 10.0 | ns |
| $t_{PHZ}$ | Output Disable Time | 5.0 | 2.0 | 7.0 | 10.5 | 1.5 | 11.5 | ns |
| $t_{PLZ}$ | Output Disable Time | 5.0 | 2.0 | 5.5 | 8.5 | 1.5 | 9.0 | ns |

**Note 9:** Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements for ACT

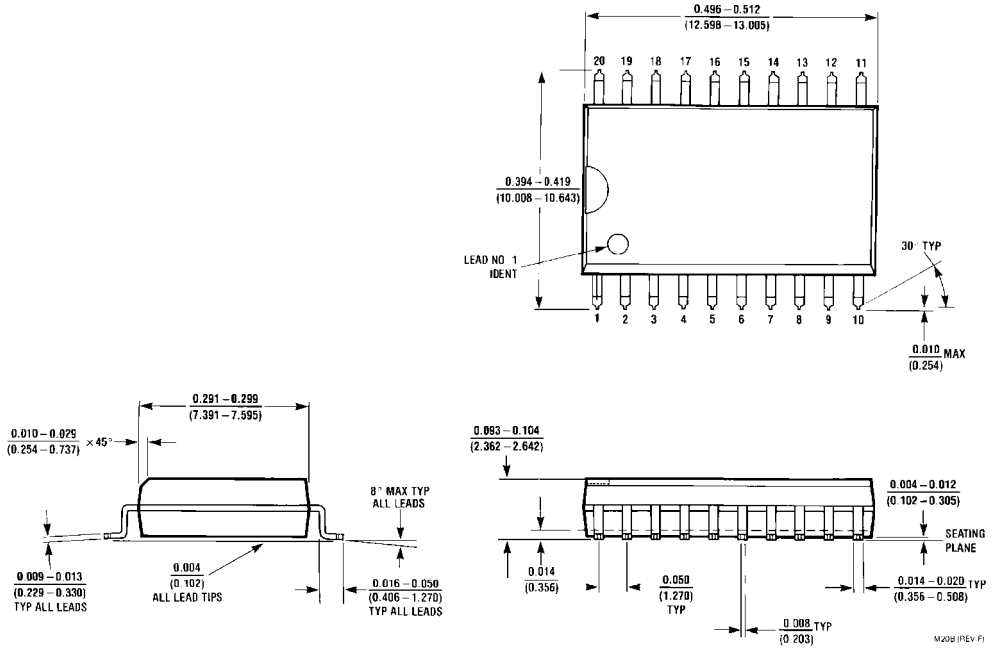
| Symbol | Parameter | $V_{CC}$ (V) (Note 10) | $T_A = +25°C$, $C_L = 50$ pF | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | Units |
|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | |
| $t_S$ | Set-Up Time, HIGH or LOW $D_n$ to CP | 5.0 | 1.5 | 2.5 | ns |
| $t_H$ | Hold Time, HIGH or LOW $D_n$ to CP | 5.0 | −0.5 | 1.0 | ns |
| $t_W$ | CP Pulse Width HIGH or LOW | 5.0 | 2.5 | 4.0 | ns |

**Note 10:** Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

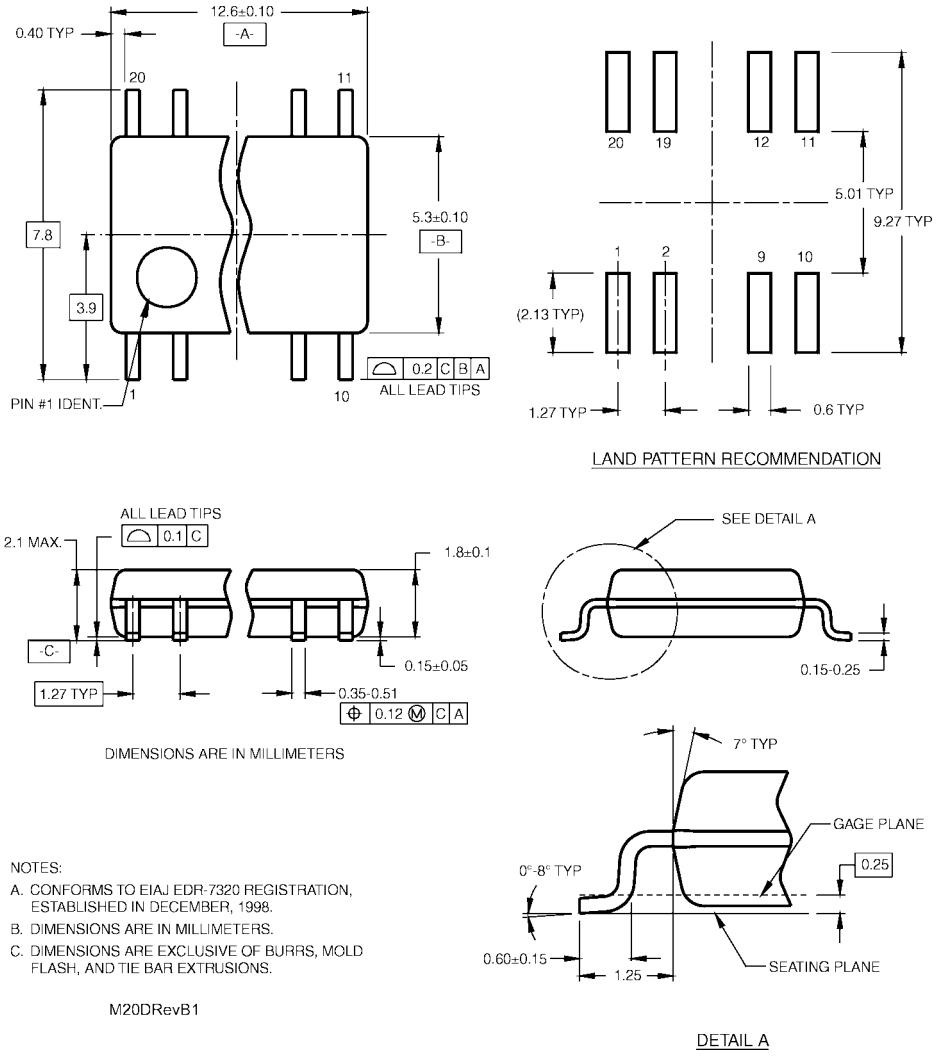
| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 40.0 | pF | $V_{CC}$ = 5.0V |

## Physical Dimensions inches (millimeters) unless otherwise noted




**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide Body**
**Package Number M20B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

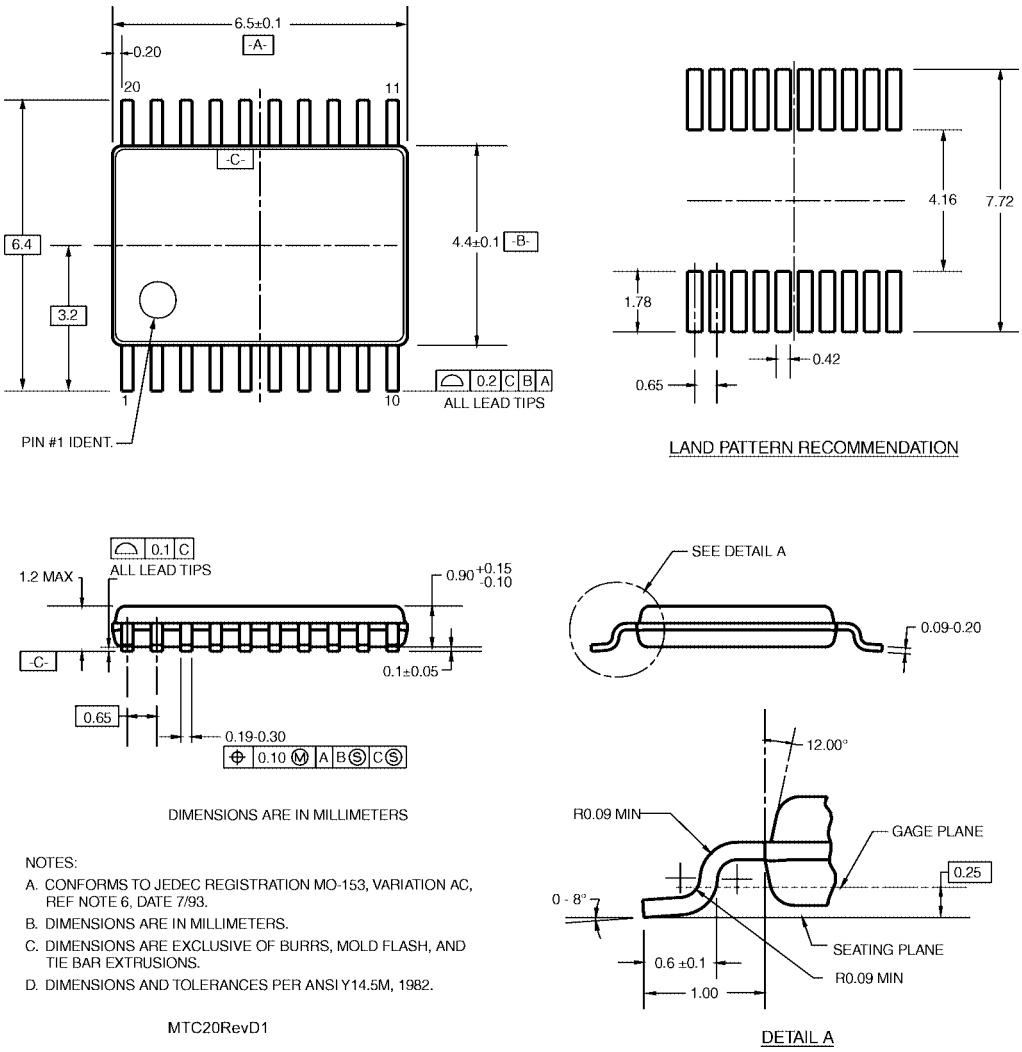
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ Type II 5.3mm Wide**
**Package Number M20D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

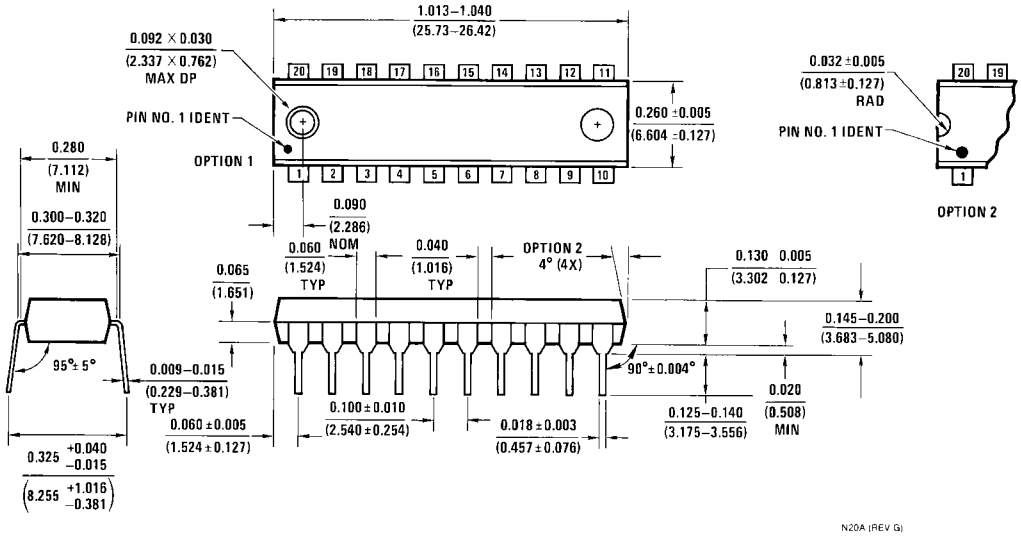
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC20**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**www.fairchildsemi.com**